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apparent limits, possible extensions, and applications of CMOS technology in the nanometer regime. Starting from device scaling theory and current industry projections, we analyze the achievable performance and

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possible limits of CMOS  
technology from the point of  
view of device physics,  
device technology, and power  
consumption.

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Nanotechnology promises to open up new ways of scaling CMOS circuits by introducing new materials. For example, a hybrid circuit of CMOS gates and carbon nano-tubes (CNT), NEMS relay logic and emerging memory devices have

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been proposed for future  
nano-scale Field  
Programmable Gate Arrays  
(FPGAs).

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Abstract: Steep subthreshold swing transistors based on interband tunneling are examined toward extending the performance of electronics systems. In particular, this review

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introduces and summarizes progress in the development of the tunnel field-effect transistors (TFETs) including its origin, current experimental and theoretical performance relative to the metal-oxide-



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ABSTRACT CMOS technology  
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regime now. The technology scaling is no longer just about geometric reduction but more about innovation in the use of new materials and transistor architectures.

**Circuit Design in Nano-Scale**

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